CLAIMS

What is claimed is:

1. A high frequency peak detector comprises:

an operational amplifier having a first inverting input, a second inverting input, a non-inverting input and an output, wherein the first inverting input is operably coupled to receive a high frequency input signal, the second inverting input is operably coupled to receive a common mode voltage of the high frequency signal, and wherein the non-inverting input is operably coupled to the output of the operational amplifier;

a transistor having a gate, a drain, and a source, wherein the gate of the transistor is operably coupled to the output of the operational amplifier and the source of the transistor is operably coupled to a power supply;

a capacitor having a first plate and a second plate, wherein the first plate of the capacitor is operably coupled to the drain of the transistor to provide an analog signal representing an average peak to common mode value of the high frequency signal and the second plate of the capacitor is operably coupled to a circuit ground; and

an average to peak conversion module operably coupled to determine a peak value of the high frequency signal based on the analog signal and the common mode value.

2. The high frequency peak detector of claim 1 further comprises:

a leakage current source operably coupled to parallel with the capacitor.

3. The high frequency peak detector of claim 1, wherein the operational amplifier comprises:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor provides the first inverting input;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor provides the second inverting input;

a third input transistor having a gate, a drain, and a source, wherein the gate of the third input transistor provides the non-inverting input;

a current source having a first node and a second node, wherein the first node of the current source is operably coupled to the sources of the first, second, and third input transistors and the second node of the current source is operably coupled to the circuit ground;

a first output transistor having a gate, a drain, and a source, wherein the drain of the first output transistor is operably coupled to the drains of the first and second input transistors to provide the output and the source of the first output transistor is operably coupled to the power supply; and

a second output transistor having a gate, a drain, and a source, wherein the drain of the second output transistor is operably coupled to the drain of the third input transistor, the gate of the second output transistor is coupled to the drain of the second output transistor and to the gate of the first output transistor, and the source of the second output transistor is operably coupled to the power supply.

4. The high frequency peak detector of claim 1, wherein the average to peak conversion module comprises:

a divider circuit operably coupled to convert the analog signal into a plurality of analog voltages;

a common mode scaling circuit operably coupled to provide a scaled common mode voltage of the common mode voltage; and

a plurality of comparators operably coupled to compare the plurality of analog voltages to the scaled common mode voltage to produce a digital value representing the peak value.

5. The high frequency peak detector of claim 4, wherein the divider circuit comprises:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive the analog signal and the source of the input transistor is operably coupled to the power supply;

resistive divider network having a first node, a second node, and a plurality of taps, wherein the first node of the resistor divider is operably coupled to the drain of the input transistor and the plurality of taps provides the plurality of analog voltages; and

a current source having a first node and a second node, wherein the first node of the current source is coupled to the second node of the resistive divider and the second node of the current source is operably coupled to the circuit ground.

6. The high frequency peak detector of claim 4, wherein the common mode scaling circuit comprises:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive the common mode voltage and the source of the input transistor is operably coupled to the power supply; and

a current source having a first node and a second node, wherein the first node of the current source is coupled to the drain of the input transistor to provide the scaled common mode voltage and the second node of the current source is operably coupled to the circuit ground.

7. The high frequency peak detector of claim 1, wherein the average to peak conversion module comprises:

a first analog to digital converter operably coupled to convert the analog signal into a digital signal;

a second analog to digital converter operably coupled to convert the common mode voltage into a second digital signal; and

look up table addressed by the digital signal and the second digital signal to retrieve the peak value of the high frequency signal.

8. A radio frequency integrated circuit (RFIC) comprises:

a receiver section operably coupled to convert inbound radio frequency (RF) signals into inbound data;

a transmitter section operably coupled to converter outbound data into outbound RF signals; and

a transmit signal strength indication (TSSI) module operably coupled to determine transmit power of the outbound RF signals, wherein the TSSI module includes:

an operational amplifier having a first inverting input, a second inverting input, a non-inverting input and an output, wherein the first inverting input is operably coupled to receive the outbound RF signals, the second inverting input is operably coupled to receive a common mode voltage of the outbound RF signals, and wherein the non-inverting input is operably coupled to the output of the operational amplifier;

a transistor having a gate, a drain, and a source, wherein the gate of the transistor is operably coupled to the output of the operational amplifier and the source of the transistor is operably coupled to a power supply;

a capacitor having a first plate and a second plate, wherein the first plate of the capacitor is operably coupled to the drain of the transistor to provide an analog signal representing an average peak to common mode value of the outbound RF signals and the second plate of the capacitor is operably coupled to a circuit ground; and

an average to peak conversion module operably coupled to determine a peak value of the outbound RF signals based on the analog signal and the common mode value.

9. The RFIC of claim 8, wherein the TSSI further comprises:

a leakage current source operably coupled to parallel with the capacitor.

10. The RFIC of claim 8, wherein the operational amplifier comprises:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor provides the first inverting input;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor provides the second inverting input;

a third input transistor having a gate, a drain, and a source, wherein the gate of the third input transistor provides the non-inverting input;

a current source having a first node and a second node, wherein the first node of the current source is operably coupled to the sources of the first, second, and third input transistors and the second node of the current source is operably coupled to the circuit ground;

a first output transistor having a gate, a drain, and a source, wherein the drain of the first output transistor is operably coupled to the drains of the first and second input transistors to provide the output and the source of the first output transistor is operably coupled to the power supply; and

a second output transistor having a gate, a drain, and a source, wherein the drain of the second output transistor is operably coupled to the drain of the third input transistor, the gate of the second output transistor is coupled to the drain of the second output transistor and to the gate of the first output transistor, and the source of the second output transistor is operably coupled to the power supply.

11. The RFIC of claim 8, wherein the average to peak conversion module comprises:

a divider circuit operably coupled to convert the analog signal into a plurality of analog voltages;

a common mode scaling circuit operably coupled to provide a scaled common mode voltage of the common mode voltage; and

a plurality of comparators operably coupled to compare the plurality of analog voltages to the scaled common mode voltage to produce a digital value representing the peak value.

12. The RFIC of claim 11, wherein the divider circuit comprises:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive the analog signal and the source of the input transistor is operably coupled to the power supply;

resistive divider network having a first node, a second node, and a plurality of taps, wherein the first node of the resistor divider is operably coupled to the drain of the input transistor and the plurality of taps provides the plurality of analog voltages; and

a current source having a first node and a second node, wherein the first node of the current source is coupled to the second node of the resistive divider and the second node of the current source is operably coupled to the circuit ground.

13. The RFIC of claim 11, wherein the common mode scaling circuit comprises:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive the common mode voltage and the source of the input transistor is operably coupled to the power supply; and

a current source having a first node and a second node, wherein the first node of the current source is coupled to the drain of the input transistor to provide the scaled common mode voltage and the second node of the current source is operably coupled to the circuit ground.

14. The RFIC of claim 8, wherein the average to peak conversion module comprises:

a first analog to digital converter operably coupled to convert the analog signal into a digital signal;

a second analog to digital converter operably coupled to convert the common mode voltage into a second digital signal; and

look up table addressed by the digital signal and the second digital signal to retrieve the peak value of the outbound RF signals.